UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,474	12/28/2000	Gunther Lehmann	00P0113 US	3514

48154 7590 06/29/2005

SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

et

Office Action Summary	Application No.	Applicant(s)	
	09/751,474	LEHMANN ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-9,16-20 and 28-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-9,16-18 and 28-42* is/are rejected.

7)☒ Claim(s) *19, 20, 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 33-36 and 38 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 1 discloses the source region [143] is separated from the lower counter electrode [171]. The specification never discloses the source region [143] being coupled to a lower counter electrode as claimed in claims 33 and 38.

2. Claim 16 is objected to because of the following informalities: lines 17, 21, 22, the phrase "a final low resistance state" is unclear whether it is being referred to the final low resistance state in lines 12-13. Appropriate correction is required.

3. Claims 8, 28, 29, 31-36 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8, line 16, claim 28, lines 3-4, claim 32, line 9, claim 33, lines 8-9, claim 38, line 5, the phrase "a gate oxide electrode" is unclear as to what is it. It is well known in the art that a gate electrode is formed on a gate oxide. It is believed that the phrase should rewrite as "a gate electrode".

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 6, 7, 9, 16-18, 30, 37 and 39-42 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Knall et al. (in the IDS filed on on 8/16/04) (fig. 5 of Knall et al. has an effective filing date on 4/28/00).

In regards to claim 1, Knall et al. show all the elements of the claimed invention in fig. 5. It is an apparatus, comprising: a semiconductor body [108] having on a surface thereof at least one lower antifuse [112] and at least one upper antifuse (the antifuse in level [102]) in vertically stacked relation with both such antifuses sharing a common intermediate electrode (middle and upper portions of [113]) therebetween; the lower antifuse [112] having a lower counter electrode [109] and a lower fusible insulator portion [112] defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode [109] with the common intermediate electrode; and the upper antifuse having an upper counter electrode (a middle portion of the conductor in rail 6) and an upper fusible insulator portion (the antifuse in level [102]) defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode, wherein the upper antifuse is in the form of a contact antifuse defining a conductive contact (a lower portion of the conductor in rail stack 6) interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with upper fuse element, the upper fuse element also being directly interconnected with the common intermediate

electrode; the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate activation to a final low electrical resistance state.

In regards to claim 6, Knall et al. further disclose the counter electrode [109] of at least one of the antifuses is interconnected by the corresponding fuse element [112] to the common intermediate electrode through at least one electrode extension portion (a lower portion of conductor [113]) interposed between said fuse element [51] and the common intermediate electrode (middle and upper portions of conductor [113]).

In regards to claim 7, Knall et al. further disclose the counter electrode (a middle portion of the conductor in rail stack 6) of at least one of the antifuses is interconnected by the corresponding fuse element (the antifuse in level [102]) to the common intermediate electrode through at least one electrode extension portion (a lower portion of conductor in the rail stack 6) interposed between said fuse element and the corresponding counter electrode (a middle portion of conductor in rail stack 6).

In regards to claim 9, Knall et al. further disclose the electrode extension portion (a lower portion of the conductor in rail stack 6) interposed between the upper counter electrode (a middle portion of the conductor in rail stack 6) and the upper fusible insulator portion (the antifuse in level [102]).

In regards to claim 37, Knall et al. show all the elements of the claimed invention in fig. 5. It is an apparatus, comprising: a semiconductor body [108] having a surface and overlying the surface in vertical relation: an upper contact antifuse having an upper counter electrode (a middle portion of the conductor in rail stack 6) and an upper fusible

insulator portion (the antifuse in level [102]) defining an upper fuse element of initial high electrical resistance; a common intermediate electrode [113] in direct contact the upper fusible insulator portion of said upper contact antifuse and opposing said upper counter electrode; and a lower contact antifuse [112] having a lower counter electrode [109] and a lower fusible insulator portion [112] defining a lower fuse element of initial high electrical resistance and interconnecting the lower counter electrode with the common intermediate electrode; the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate activation to a final low electrical resistance state.

In regards to claim 39, Knall et al. inherently teach upper and lower activation circuitry for selectively energizing the upper and lower antifuses separately because all the memory device would require a decoder circuitry and a programming circuitry to select and activate the memory elements (paragraph [0028]).

In regards to claim 40, Knall et al. show the upper antifuse is in the form of a direct contact antifuse defining a conductive contact (a lower portion of the conductor in rail stack 6) interposed between the upper counter electrode (a middle portion of the conductor in rail stack 6) and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with upper fuse element.

In regards to claims 16, 41, Knall et al. show all the elements of the claimed invention in fig. 5. It is an apparatus, comprising: a semiconductor body [108] having on a surface thereof at least one lower antifuse [112] and at least one upper antifuse (the antifuse in level [102]) in vertically stacked relation with both such antifuses sharing a

common intermediate electrode [113] therebetween; the lower antifuse [112] having a lower counter electrode [109] and a lower fusible insulator portion [112] defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode [109] with the common intermediate electrode [113]; and the upper antifuse having an upper counter electrode (a middle portion of the conductor in rail stack 6) and an upper fusible insulator portion (the antifuse in level [102]) defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode [113]; the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate activation to a final low electrical resistance state; and it inherently further comprising energizable fuse activation circuit means (decoder circuitry and programming circuitry are well known circuitry in memory device like Knall et al. to activate the memory cells (paragraph [0028])) defining a lower fuse activation circuit for applying and controlling a selective blow voltage across the lower counter electrode and common intermediate electrode at the lower fuse element for fusibly blowing the lower antifuse to a final low electrical resistance state to interconnect electrically conductively the lower counter electrode and the common intermediate electrode thereat, and further defining an upper fuse activation circuit for applying and controlling a selective blow voltage across the upper counter electrode and common intermediate electrode at the upper fuse element for fusibly blowing the upper antifuse to a final low electrical resistance state to interconnect electrically conductively the upper counter electrode and the common intermediate electrode thereat.

In regards to claim 17, Knall et al. inherently further disclose unblown or blown fuse activation state sensing and indicating circuit means (sensing and indicating circuits are well known circuits in memory device to sense and indicate the state of the memory in the memory cells (paragraph [0028])) defining a lower fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the lower antifuse, and further defining an upper fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the upper antifuse.

In regards to claim 18, Knall et al. further inherently disclose the fuse activation circuit means are arranged for independently applying and controlling a selective blow voltage for fusibly blowing the lower antifuse, and for independently applying and controlling a selective blow voltage for fusibly blowing the upper antifuse, to permit their respective selective energizing for corresponding separate fuse activation.

In regards to claim 30, Knall et al. further disclose the upper antifuse is in the form of a contact antifuse defining a conductive contact (a lower portion of the conductor in rail 6) interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with upper fuse element, the upper fuse element also being directly interconnected with the common intermediate electrode.

In regards to claim 42, Knall et al. further inherently disclose the upper and lower fuse activation circuits may energize the upper and lower fusible insulator portions separately.

6. Claim 8 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

7. Claims 19, 28, 31, 32 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 19, 20 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is the lower antifuse is in the form of a gate oxide antifuse having a source region and a drain region. The second major difference in the claims not found in the prior art of record is the upper and lower fuse activation circuits may energize the upper and lower fusible insulator portions simultaneously.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
June 26, 2006

Steven Loke
Primary Examiner